REMARKS

I. Introduction

In response to the Office Action dated April 3, 2006, claims 1, 13, 14, and 16 have been amended. Claims 1-22 remain in the application. Re-examination and reconsideration of the application, as amended, are respectfully requested.

II. Claim Amendments

Applicants' attorney has made amendments to the claims as indicated above. These amendments were made solely for the purpose of clarifying the language of the claims, and were not required for patentability or to distinguish the claims over the prior art.

III. Prior Art Rejections

In paragraphs (1)-(2) of the Office Action, claims 1-3, 9-15, and 20-21 were rejected under 35 U.S.C. §102(b) as being anticipated by Carlson, U.S. Patent No. 4,833,479 (Carlson). On page (6), paragraph (1) of the Office Action, claims 4-8 were rejected under 35 U.S.C. §103(a) as being unpatentable over Carlson in view of Nakamura et al., U.S. Patent No. 6,275,520 (Nakamura). On page (7), paragraphs (2)-(3) of the Office Action, claims 16-19 and 22 were rejected under 35 U.S.C. §102(e) as being anticipated by Oishi et al., U.S. Patent No. 6,650,689 (Oishi).

Applicants respectfully traverse these rejections in light of the amendments above and the arguments presented herein.

The Carlson Reference

Carlson merely describes a digital poly phase pulse compressor that utilizes delay lines to separate KN samples of a received compressed pulse in I and Q channels, multiplies N of the KN samples with quadrature, weighted code phase signals by shifting and adding, cross couples the products of the shifting and adding in the I and Q channels to remove all code phase terms from the N samples in each channel, and combines the final n signals to provide I and Q compressed pulse components. The I and Q channels can be expanded into pluralities of channels to include compensation for Dopplet shift.

The Nakamura Reference

Nakamura merely describes a pseudo-noise generating apparatus capable of starting a pseudo-noise sequence from an arbitrary phase using compact processing circuitry. Tap selection patterns corresponding to a plurality of phase shift amounts are stored in advance in a ROM. By giving a phase shift amount to the ROM and setting the corresponding tap selection pattern in AND gates, the pseudo-noise sequence generated by the pseudo-noise generator is shifted in phase, and is loaded into a shift register. After setting a new phase amount in the ROM, the contents of the shift register are transferred into a shift register in the pseudo-noise generator. By repeating this operation, the desired phase shift is accomplished as a sum of a plurality of phase shift amounts.

The Oishi Reference

Oishi merely describes an invention which reduces the scale of circuitry and shortens the code phase detection time needed to achieve initial synchronization. In a correlator for calculating correlation between a received spreading code contained in a received spread-spectrum signal and a reference spreading code, a combined code generator is included. The combined code generator outputs a combined spreading code by weighting and combining a plurality of phase-shifted reference spreading codes A.sub.1 -A.sub.M. Further, an arithmetic circuit calculates correlation between the received spreading code and the plurality of phase-shifted reference spreading codes simultaneously. A phase detection circuit detects the phase difference between the received spreading code and a reference spreading code, namely the phase of the received spreading code from the results of the arithmetic operation.

The Claims are Patentable Over the Cited References

Independent claims 1, 13, and 16 are generally directed to a device for generating at least one code phase. Such a device comprises a shift register comprising N outputs and an input to which a code sequence is applied, N being an integer greater than two, and at least one logic branch, controlled by at least one combination control signal, on the basis of which the logic branch combines the code phase from i outputs of the shift register simultaneously, i being an integer between 2 and N, wherein said combination control signal is usable to set one or more weighting coefficients.

The cited references do not teach nor suggest these various elements of Applicants' independent claims. Specifically, the cited references do not teach or suggest at least the limitations of applying a code sequence to the shift register and the logic branch combining the code phase from i outputs of the shift register simultaneously, i being an integer between 2 and N as recited in the claims of the present invention.

Referring specifically to FIG. 1 of Carlson, a receiver 10 supplies an IF signal to inputs of two mixers 12 and 14. A second input of mixer 12 is connected through a ninety degree phase shifting circuit 15 to the output of a coherent local oscillator 16, which output is also connected directly to a second input of mixer 14. The quadrature baseband analog signals from mixers 12 and 14 are supplied through amplifiers to in-phase (I) and quadrature (Q) analog-to-digital (A/D) converters 18 and 20, respectively. The digital signals from A/D converters 18 and 20 are supplied to two N stage delay lines 22 and 24, respectively. A pulse compression ratio of N implies the existence of an N-stage delay line in each channel. The digital samples from each stage of the N stage delay lines 22 and 24 are coupled to separate multiply and add circuits, only one of which is illustrated in FIG. 1, for convenience, and is illustrated as being coupled to the i th stages of delay lines 22 and 24.

The multiply and add circuit of FIG. 1 includes two correlator networks 25 and 30 each having two multipliers 26,27 and 28,29, respectively, two adding circuits 32 and 33, and two summation circuits 35 and 36. The output from the i th stage of I delay line 22 is connected to first inputs of multiplier 26 and multiplier 27. The output from the i th stage of Q delay line 24 is connected to first inputs of multipliers 28 and 29. Quadrature code phase signals are stored in a storage device 40. A first signal, sin θ_{c_i}, is connected to second inputs of multipliers 27 (negatively) and 28. A second signal from storage device 40, cos θ_{c_i}, is connected to second inputs of multipliers 26 and 29. The output of multiplier 26 and the matching output of multiplier 28 are cross coupled to inputs of adding circuit 32. The output of multiplier 29 and the matching output of multiplier 27 are cross coupled to inputs of adding circuit 33. The outputs of adding circuits 32 and 33 are connected to summing circuits 35 and 36, respectively. The N samples from each of the adding circuits coupled to I delay line 22 are linearly summed in summation circuit 35 and the N samples from each of the adding circuits coupled to Q delay line 24 are linearly summed in summation circuit 36. See Carlson, Col. 2, line 42-Col. 3, line 17.

In the present invention, the logic branch combines the code phase from i outputs of the shift register simultaneously, i being an integer between 2 and N. Carlson, in contrast, takes an output from the shift register serially, rather than taking at least two outputs from the shift register simultaneously. In other words, Carlson does not show that shift register 22 has multiple taps going to, for example, multiplier 27. As such, Carlson does not show the limitation of the logic branch combining the code phase from i outputs of the shift register simultaneously, i being an integer between 2 and N as recited in the claims of the present invention.

Further, Carlson discusses performing shift register operations on a digitized receive signal, i.e., the IF signal received by receiver 10. The present invention claims a code sequence, not a digitized receive signal

The ancillary Nakamura and Oishi references do not remedy the deficiencies of the Carlson reference. Specifically, Nakamura and Oishi, alone, or in any combination with Carlson, do not teach or suggest at least the limitation of the logic branch combines the code phase from i outputs of the shift register simultaneously, i being an integer between 2 and N as recited in the claims of the present invention.

Moreover, the various elements of Applicants' claimed invention together provide operational advantages over Carlson, Nakamura, and Oishi. In addition, Applicants' invention solves problems not recognized by Carlson, Nakamura, and Oishi.

Thus, Applicants submit that independent claims 1, 13, and 16 are allowable over Carlson and Nakamura. Further, dependent claims 2-12, 14-15, and 17-22 are submitted to be allowable over Carlson, Nakamura, and Oishi in the same manner, because they are dependent on independent claims 1, 13, and 16, respectively, and thus contain all the limitations of the independent claims. In addition, dependent claims 2-12, 14-15, and 17-22 recite additional novel elements not shown by Carlson, Nakamura, and Oishi.

IV. Conclusion

In view of the above, it is submitted that this application is now in good order for allowance and such allowance is respectfully solicited. Should the Examiner believe minor matters still remain that can be resolved in a telephone interview, the Examiner is urged to call Applicants' undersigned attorney.

Respectfully submitted,

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